CLAIMS:

1. A microelectronic chip assembly comprising at least three microelectronic chips that are stacked together, at least one of the chips, denoted intermediate chip, comprising via holes filled with conductive material running through said chip, characterized in that said intermediate chip is realized from a high-ohmic substrate comprising devices to be used by at least two other microelectronic chips, called top and bottom chips, arranged on at least one face of said intermediate chip, said top and bottom chips being connected by flip chip bonding on top and bottom faces of said intermediate chip, respectively, said via holes realizing an electrical connection between pads of said top and bottom chips.

2. An assembly as claimed in Claim 1, wherein said intermediate chip, which is also linked by flip chip bonding to an external connection device, makes the connection with external circuits possible.

3. An assembly as claimed in Claim 2, wherein high and low- performance sensitive devices are integrated on said bottom, intermediate and top chips in order that said devices are stacked in a specific order relative to said connection device, said specific order being such that high- performance sensitive devices are integrated on the bottom chip and low-performance sensitive devices are integrated on the top chip.

4. An assembly as claimed in one of the Claims 2 and 3, wherein said connection device includes a heatsink dedicated to realize a contact with said bottom chip.

5. An assembly as claimed in Claim 4, wherein at least a heat dissipative device is integrated on said bottom chip, said bottom chip realizing a contact with said heat-sink.

6. An assembly as claimed in Claim 4, wherein at least a high-frequency device is integrated on said bottom chip, said bottom chip being in contact with said heatsink.

7. An assembly as claimed in one of the Claims 1 and 2, wherein said intermediate chip comprises integrated devices on both sides.

8. A packaged system including at least three devices that are integrated on separate chips, characterized in that said chips are arranged in an assembly as claimed in one of the claims 1 to 7.

9. A method of manufacturing a miniaturized packaged system including at least a microelectronic assembly, characterized in that said method includes the steps of:

- Realizing at least one chip from a high-ohmic substrate, called intermediate chip, including integrated devices on at least one face and via holes running through said chip and filled with conductive material,
- Linking at least one chip, called bottom chip, including integrated devices on one face, by flip chip bonding on said intermediate chip, in order that said via holes are connected with terminal pads of said bottom chip,
- Linking the intermediate chip by flip chip bonding on a connection device in order that said bottom chip is stacked between said intermediate chip and said connection device,
- Linking by flip chip bonding a third chip, called top chip, including integrated devices on one face, on said intermediate chip, in order that said via holes are in connection with terminal pads of said top chip,
- Molding the assembly in a molding component.